Express Mail Label No. EL975549382US

PATENTS
Docket No. BUR920010034US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Leendert M. Huisman, William V. Huott, Franco Motika and Leah M. Pfeifer Pastel
Serial No.	:	(unknown)
Filed	:	Herewith
For	:	USING CLOCK GATING OR SIGNAL GATING TO PARTITION A DEVICE FOR FAULT ISOLATION AND DIAGNOSTIC DATA COLLECTION
Group Art Unit	:	(unknown)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicants wish to call the attention of the Examiner to the following references:

U.S. Patent No. 4,509,008 DasGupta et al.

U.S. Patent No. 4,800,564 DeFazio et al.

U.S. Patent No. 5,119,378 Welles, II et al.

U.S. Patent No. 5,132,974 Rosales

U.S. Patent No. 6,125,465 McNamara et al.

U.S. Patent No. 6,536,024 Hathaway

C.J. Richard Shi, "Block-Level Fault Isolation Using Partition Theory and Logic Minimization Techniques"

March 1997, ECE Department, University of Iowa, Iowa City, Iowa 52242.

These references also are listed on the accompanying Information Disclosure Statement (Form PTO-1449). Because copies of these references are readily available from parent application U.S. Serial No. 09/930,355, filed August 15, 2001, copies of the references are not enclosed herewith. Should the Examiner wish to receive copies of these references, Applicants will provide the same. The submission of this Information Disclosure Statement shall not be construed as a representation that a search has been made or that no other art than that identified above exists.

Consideration of the foregoing in relation to this patent application is respectfully requested.

Respectfully Submitted,

Brian M. Dugan, Esq.
Registration No. 41,720
Attorney for Applicants
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Dated: October 30, 2003
Tarrytown, New York

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. BUR920010034US2	SERIAL NO. (unknown)
	APPLICANTS :Leendert M. Huisman, William V. Huott, Franco Motika and Leah M. Pfeifer Pastel	
(Use several sheets if necessary)	FILING DATE: Herewith	GROUP: (unknown)

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	AA	4,509,008	Apr. 2, 1985	DasGupta et al.			
	AB	4,800,564	Jan. 24, 1989	DeFazio et al.			
	AC	5,119,378	Jun. 2, 1992	Welles, II et al.			
	AD	5,132,974	Jul. 21, 1992	Rosales			
	AE	6,125,465	Sep. 26, 2000	McNamara et al.			
	AF	6,536,024	Mar.18, 2003	Hathaway			
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ		C.J. Richard Shi, "Block-Level Fault Isolation Using Partition Theory and Logic Minimization Techniques" March 1997, ECE Department, University of Iowa, Iowa City, Iowa 52242, USA

EXAMINER | DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.